Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"6769050".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:26
L2	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L3	16624	first adj port and second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L4	1378755	port or ports or interface or i/f or interfaces	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L5	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L6	28395	first adj mode and second adj mode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L7	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:29
L8	229201	memory near4 access	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L9	128378	(memory adj core) or bank	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L10	15193	first adj port same second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L11	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L12	5	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L13	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L14	13	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L15	5	(memory adj controller) and (first adj port and second adj port) and (port or ports or interface or i/f or interfaces) and (memory adj core) and (first adj mode and second adj mode) and (memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L16	5	(memory adj controller) and (first adj port and second adj port) and (memory adj core) and (first adj mode and second adj mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L17	7	(memory adj controller) and (first adj port and second adj port) and (first adj mode and second adj mode) and core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L18	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L19	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L20	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L21	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L22	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L23	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L24	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L25	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L26	863	365/230.05.cds.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

					т	
L27	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L28	18	((memory near4 access) and (first adj port same second adj port)) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L29	11	single adj port adj memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L30	8	(((memory near4 access) and (first adj port same second adj port)) and (memory adj core)) and (single adj port adj memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L31	583	single adj port adj memory	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L32	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L33	3	711/163.ccls. and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L34	6	711/149.ccls. and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L35	1	"5130981".PN.	USPAT	OR	OFF	2005/01/21 18:30
L36	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L37	16624	first adj port and second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L38	1378755	port or ports or interface or i/f or interfaces	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L39	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L40	28395	first adj mode and second adj mode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L41	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

Search History 1/21/05 6:49:28 PM Page 3 C:\APPS\EAST\Workspaces\10862375.wsp

L42	229201	memory near4 access	US-PGPUB;	OR	OFF	2005/01/21 18:30
L 12	223201	memory near racess	USPAT; EPO; JPO; IBM_TDB			
L43	128378	(memory adj core) or bank	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L44	15193	first adj port same second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L45	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L46	5	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L47	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L48	13	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L49	5	(memory adj controller) and (first adj port and second adj port) and (port or ports or interface or i/f or interfaces) and (memory adj core) and (first adj mode and second adj mode) and (memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L50	5	(memory adj controller) and (first adj port and second adj port) and (memory adj core) and (first adj mode and second adj mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L51	7	(memory adj controller) and (first adj port and second adj port) and (first adj mode and second adj mode) and core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L52	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L53	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L54	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

			LIC DCDLID.	00	٥٢٢	2005/01/21 10:20
L55	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L56	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L57	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L58	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L59	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L60	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L61	863	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L62	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L63	18	((memory near4 access) and (first adj port same second adj port)) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L64	8	(((memory near4 access) and (first adj port same second adj port)) and (memory adj core)) and (single adj port adj memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L65	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L66	1397618	simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L67	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L68	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L69	13	((memory adj controller) same (first adj port same	US-PGPUB;	OR	OFF	2005/01/21 18:30
		second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	USPAT; EPO; JPO; IBM_TDB			
L70	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TD8	OR	OFF	2005/01/21 18:30
L71	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L72	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L73	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L74	5	((memory adj controller) same (first adj port same second adj port)) and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L75	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L76	9	(memory adj controller) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L77	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L78	5	(((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L79	5	((memory adj controller) same (first adj port same second adj port)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L80	9	(memory adj controller) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L81	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L82	26	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and (first adj port and second adj port and third adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L83	18	single adj port near2 core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L84	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and (((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L85	9	(single adj port near2 core) and (((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access)) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and ((((memory near4 access)) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L86	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L87	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L88	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L89	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L90	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L91	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

			<u> </u>	T	T	
L92	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L93	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L94	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L95	863	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L96	9189	711/149.ccls. or 711/163.ccls. or 711/173.ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03. ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L97		((memory adj controller) same (first adj port same second adj port)) and (711/149.ccls. or 711/163. ccls. or 711/173.ccls. or 711/154.ccls. or 365/189. 02.ccls. or 365/189.03.ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230. 05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L98	53	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and (711/149.ccls. or 711/163.ccls. or 711/173. ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03.ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230.05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L99	49	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2) and (711/149.ccls. or 711/163.ccls. or 711/173.ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03.ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230.05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L100	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L101	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L102	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L103	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L104	11	(memory adj controller) same (first adj port same second adj port same third adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L105	5	(US-6633296-\$ or US-6625687-\$ or US-6546449-\$ or US-6480946-\$).did. or (US-20040019748-\$).did.	US-PGPUB; USPAT	OR	OFF	2005/01/21 18:30
L106	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L107	1	L105 and L106	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L108	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L109	5	L100 and L101 and L102	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L110	5	L108 and L109	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L111	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L112	294	711/149.cds.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L113	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L114	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L115	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L116	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L117	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

						, , , , , , , , , , , , , , , , , , , ,
L118	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L119	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L120	3589	L111 or L112 or L113 or L114	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L121	8685	L115 or L116 or L117 or L118 or L119 or L120	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L122	92	L100 and L102	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L123	10	L120 and L122	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L124	10	L121 and L122	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR /	OFF	2005/01/21 18:30
L125	10	L123 or L124	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L126	11826100	@ad<"20010910"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L127	4	L125 and L126	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L128	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L129	16624	first adj port and second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L130	1378755	port or ports or interface or i/f or interfaces	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L131	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L132	28395	first adj mode and second adj mode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L133	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR .	OFF	2005/01/21 18:30
L134	229201	memory near4 access	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L135	128378	(memory adj core) or bank	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L136	15193	first adj port same second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF .	2005/01/21 18:30
L137	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L138	5	(memory adj controller) and (first adj port and second adj port) and (port or ports or interface or i/f or interfaces) and (memory adj core) and (first adj mode and second adj mode) and (memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L139	5	(memory adj controller) and (first adj port and second adj port) and (memory adj core) and (first adj mode and second adj mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR .	OFF	2005/01/21 18:30
L140	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L141	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L142	759 ·	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L143	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L144	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

		· · · · · · · · · · · · · · · · · · ·	·	,		
L145	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L146	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L147	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L148	863	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L149	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L150	11	single adj port adj memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L151	583	single adj port adj memory	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L152	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L153	3	711/163.ccls. and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L154	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L155	16624	first adj port and second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L156	1378755	port or ports or interface or i/f or interfaces	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L157	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L158	28395	first adj mode and second adj mode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L159	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L160	229201	memory near4 access	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L161	128378	(memory adj core) or bank	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L162	15193	first adj port same second adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L163	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L164	5	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L165	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L166	13	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L167	5	(memory adj controller) and (first adj port and second adj port) and (port or ports or interface or i/f or interfaces) and (memory adj core) and (first adj mode and second adj mode) and (memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L168	5	(memory adj controller) and (first adj port and second adj port) and (memory adj core) and (first adj mode and second adj mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L169	7	(memory adj controller) and (first adj port and second adj port) and (first adj mode and second adj mode) and core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L170	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L171	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

		T	1	1		
L172	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L173	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L174	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L175	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L176	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L177	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L178	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L179	863	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L180	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L181	18	((memory near4 access) and (first adj port same second adj port)) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR [*]	OFF	2005/01/21 18:30
L182	8	(((memory near4 access) and (first adj port same second adj port)) and (memory adj core)) and (single adj port adj memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L183	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L184	1397618	simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L185	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L186	36193	memory adj controller	US-PGPUB; USPAT;	OR	OFF	2005/01/21 18:30
			EPO; JPO; IBM_TDB			
L187	13	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L188	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L189	100	((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L190	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L191	1714	(memory near4 access) and (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L192	5	((memory adj controller) same (first adj port same second adj port)) and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L193	81	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L194	9	(memory adj controller) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L195	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L196	5	(((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L197		((memory adj controller) same (first adj port same second adj port)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

			····			
L198	9	(memory adj controller) and (((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L199	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L200	26	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and (first adj port and second adj port and third adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L201	18	single adj port near2 core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L202	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L203	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR .	OFF	2005/01/21 18:30
L204	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L205	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L206	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L207	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L208	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L209	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

L210	661	365/230.02.ccls.	US-PGPUB;	OR	OFF	2005/01/21 18:30
			USPAT; EPO; JPO; IBM_TDB			
L211	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L212	863	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L213	9189	711/149.ccls. or 711/163.ccls. or 711/173.ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03. ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L214	8	((memory adj controller) same (first adj port same second adj port)) and (711/149.ccls. or 711/163. ccls. or 711/173.ccls. or 711/154.ccls. or 365/189. 02.ccls. or 365/189.03.ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230. 05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L215	53	(((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and (711/149.ccls. or 711/163.ccls. or 711/173. ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03.ccls. or 365/189.04.ccls. or 365/230.02.ccls. or 365/230.03.ccls. or 365/230.05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L216	49	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2) and (711/149.ccls. or 711/163.ccls. or 711/173.ccls. or 711/154.ccls. or 365/189.02.ccls. or 365/189.03.ccls. or 365/230.03.ccls. or 365/230.05.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L217	36193	memory adj controller	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L218	2455	memory adj core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L219	6169	first adj port and second adj port and third adj port	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L220	62	(memory adj controller) same (first adj port same second adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L221	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

					·	
L222	81	((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L223	5	L217 and L218 and L219	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L224	1686	711/154.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L225	294	711/149.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L226	1051	711/163.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L227	759	711/173.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L228	770	365/189.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L229	237	365/189.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L230	914	365/189.04.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L231	661	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L232	3313	365/230.03.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L233	3589	L224 or L225 or L226 or L227	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L234	8685	L228 or L229 or L230 or L231 or L232 or L233	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L235	92	L217 and L219	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

-L236	10	L233 and L235	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L237	10	L234 and L235	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L238	10	L236 or L237	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L239	11826100	@ad<"20010910"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L240	1	"5130981".PN.	USPAT	OR	OFF	2005/01/21 18:30
L241	5	(US-6633296-\$ or US-6625687-\$ or US-6546449-\$ or US-6480946-\$).did. or (US-20040019748-\$).did.	US-PGPUB; USPAT	OR	OFF	2005/01/21 18:30
L242	1	L241 and L221	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L243	5	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L244	10	(first adj mode and second adj mode) and ((memory adj controller) same (first adj port same second adj port))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L245	13	((memory adj controller) same (first adj port same second adj port)) and (port or ports or interface or i/f or interfaces) and ((memory adj core) or bank)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L246	7	(memory adj controller) and (first adj port and second adj port) and (first adj mode and second adj mode) and core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L247	18	((memory near4 access) and (first adj port same second adj port)) and (memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L248	8	(((memory near4 access) and (first adj port same second adj port)) and (memory adj core)) and (single adj port adj memory adj core)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L249	6	711/149.ccls. and (((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30

		,				
L250	9	(single adj port near2 core) and (((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2)) and ((((memory near4 access) and (first adj port same second adj port)) and (single adj port adj memory)) and simultaneous\$2) and ((memory near4 access) and (first adj port same second adj port))))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L251	. 11	(memory adj controller) same (first adj port same second adj port same third adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:44
L252	5	(US-6633296-\$ or US-6625687-\$ or US-6546449-\$ or US-6480946-\$).did. or (US-20040019748-\$).did.	US-PGPUB; USPAT	OR	OFF	2005/01/21 18:30
L253	5	L222 and L223	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L254	4	L238 and L239	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:30
L255	4	239 and 251	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:45
L256	444	access\$3 near3 (first adj2 interface)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:46
L257	0	255 and 256	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:46
L258	66	(multi-port or multiport) near3 module?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:46
L259	11029	(first adj2 interface) and (second adj2 interface)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:47
L260	3	258 and 259	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:47
L261	3	260 and 239	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:48
L262	28395	(first adj mode) and (second adj mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/01/21 18:48

L263	1	258 and 262	US-PGPUB;	OR	OFF	2005/01/21 18:49
			USPAT;			
			EPO; JPO;			
			IBM_TDB			



Publications/Services Standards Conferences Careers/Jobs Membership

Welcome **United States Patent and Trademark Office**

A	RELEASE 1.0
Help FAQ Terms IEEE	Peer Review Quick Links
Welcome to IEEE Xplore® - Home - What Can I Access? - Log-out Tables of Contents	Your search matched 0 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering in the text box.
 Journals & Magazines Conference Proceedings Standards 	'multiport module' <and> interface <and> 'memory core Search Check to search within this result set Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard</and></and>
Search - By Author - Basic - Advanced - CrossRef	Results: No documents matched your query.
Member Services - Join IEEE - Establish IEEE - Web Account - Access the	

Print Format

IEEE Enterprise

— Access the

IEEE Member Digital Library

IEEE Enterprise File Cabinet

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top



IEEE Xplore®

Welcome
United States Patent and Trademark Office

	RELEASE 1.8
Help FAQ Terms IEEE F	Peer Review Quick Links
Welcome to IEEE Xplore® - Home - What Can I Access? - Log-out	Your search matched 0 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering
Tables of Contents	in the text box. multiport module <and> memory core Search</and>
O- Journals & Magazines O- Conference Proceedings O- Standards	multiport module <and> memory core Check to search within this result set Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard</and>
Search	
O- By Author O- Basic O- Advanced O- CrossRef	Results: No documents matched your query.
Member Services - Join IEEE - Establish IEEE - Web Account - Access the - IEEE Member - Digital Library	
IEEE Enterprise	

Print Format

O Access the

IEEE Enterprise File Cabinet

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top



Publications/Services Standards Conferences Careers/Jobs Membership

Welcome **United States Patent and Trademark Office**

	RELEASE 1.8
Help FAQ Terms IEEE I	Peer Review Quick Links
Welcome to IEEE Xplore® - Home - What Can I Access? - Log-out Tables of Contents	Your search matched 0 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering in the text box. Multiport module <and> simultaneous</and>
O- Journals & Magazines	Check to search within this result set
Conference Proceedings Standards	Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard
Search	·
O- By Author O- Basic O- Advanced O- CrossRef	Results: No documents matched your query.
Member Services	
O- Join IEEE O- Establish IEEE Web Account O- Access the IEEE Member Digital Library	
IEEE Enterorise	

Print Format

O- Access the

IEEE Enterprise File Cabinet

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top



Publications/Services Standards Conferences Careers/Jobs Membership Welcome **United States Patent and Trademark Office** Help FAQ Terms IEEE Peer Review **Quick Links** Welcome to IEEE Xplore® Your search matched 0 of 1117580 documents. O- Home A maximum of 500 results are displayed, 15 to a page, sorted by Relevance)- What Can **Descending** order. I Access? **Refine This Search:** O- Log-out You may refine your search by editing the current search expression or enterin in the text box. Tables of Contents multiport module <and> 'simultaneous access' Search — Journals & Magazines L. Check to search within this result set Conference **Proceedings Results Key: JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard O- Standards Search O- By Author **Results:** No documents matched your query. - Basic O- Advanced ()- CrossRef **Member Services** O- Join IEEE

IEEE Enterprise

— Access the **IEEE Enterprise** File Cabinet

)- Establish IEEE Web Account

)- Access the **IEEE Member** Digital Library

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

IEEE HOME ! SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE Standards Conferences Careers/Jobs Membership Publications/Services Welcome United States Patent and Trademark Office Help FAQ Terms IEEE Peer Review **Quick Links** Welcome to IEEE Xplore® Your search matched **20** of **1117580** documents. ()- Home A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance**)- What Can **Descending** order. I Access? C Log-out **Refine This Search:** You may refine your search by editing the current search expression or enterin Tables of Contents in the text box. Search memory <and> simultaneous access ()- Journals & Magazines L Check to search within this result set)- Conference **Proceedings Results Key:** JNL = Journal or Magazine CNF = Conference STD = Standard Standards Search 1 Dynamic access load balancing on the parallel secondary storage By Author Kitamura, T.; Oue, Y.; Ohnishi, K.; Shimizu, M.; Parallel Algorithms/Architecture Synthesis, 1997. Proceedings. Second Aizu Int)- Basic Symposium, 17-21 March 1997 Advanced Pages:316 - 323 CrossRef [Abstract] [PDF Full-Text (620 KB)] IEEE CNF **Member Services** 2 SWEB: towards a scalable World Wide Web server on multicomputer: Andresen, D.; Tao Yang; Holmedahl, V.; Ibarra, O.H.; Parallel Processing Symposium, 1996., Proceedings of IPPS '96, The 10th Inter - Establish IEEE Web Account 19 April 1996 Pages:850 - 856 Access the **IEEE Member** [Abstract] [PDF Full-Text (716 KB)] Digital Library 3 On the cost-effectiveness of PRAMs **IEEE Enterprise** Abolassan, F.; Keller, J.; Paul, W.J.; Access the Parallel and Distributed Processing, 1991. Proceedings of the Third IEEE Sympo **IEEE Enterprise** Dec. 1991 File Cabinet Pages:2 - 9 Print Format [PDF Full-Text (604 KB)] [Abstract] 4 Multiaccess memory system for attached SIMD computer Jong Won Park:

Computers, IEEE Transactions on , Volume: 53 , Issue: 4 , April 2004

Pages:439 - 452

[Abstract] [PDF Full-Text (1700 KB)]

5 An effective memory addressing scheme for FFT processors

Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing Signal Proc IEEE Transactions on], Volume: 47, Issue: 3, March 1999 Pages:907 - 911

[Abstract] [PDF Full-Text (220 KB)] **IEEE JNL**

6 Parallel implementation of motion-compensation for HDTV video dec Lee, C.L.;

Consumer Electronics, IEEE Transactions on , Volume: 44 , Issue: 2 , May 199

Pages:251 - 255

[Abstract] [PDF Full-Text (352 KB)] IEEE JNL

7 Conflict free memory addressing for dedicated FFT hardware

Johnson, L.G.;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transaction also Circuits and Systems II: Express Briefs, IEEE Transactions on], Volume: 5, May 1992

Pages: 312 - 316

[Abstract] [PDF Full-Text (412 KB)] IEEE JNL

8 An integrated pre-access architecture for CMOS SRAM

Gunther, B.K.;

Solid-State Circuits, IEEE Journal of , Volume: 27 , Issue: 6 , June 1992

Pages:901 - 907

[Abstract] [PDF Full-Text (616 KB)] IEEE JNL

9 Instruction cache organisation for embedded low-power processors

Changwoo Jung; Jihong Kim;

Electronics Letters, Volume: 37, Issue: 9, 26 April 2001

Pages: 554 - 555

[Abstract] [PDF Full-Text (268 KB)] IEE JN1

10 The architecture of OCMP and its evaluation

Saisho, K.; Sano, T.; Fukuda, A.;

Parallel Architectures, Algorithms, and Networks, 1997. (I-SPAN '97) Proceedir International Symposium on , 18-20 Dec. 1997

Pages:71 - 77

[Abstract] [PDF Full-Text (652 KB)] IEEE CNF

11 Parallel implementation of motion-compensation for HDTV video de

Lee, C.L.;

ISCE '97 - Proceedings of 1997 IEEE International Symposium on Consumer El 4 Dec. 1997

Pages:51 - 54

[Abstract] [PDF Full-Text (280 KB)] IEEE CNF

12 A distributed cache memory for multiprocessors based on the crossi interconnection principle

Lindig Bos, M.;

Circuits and Systems, 1996., IEEE 39th Midwest symposium on , Volume: 1 , 1 1996

Pages:77 - 80 vol.1

[Abstract] [PDF Full-Text (420 KB)] IEEE CNF

13 A multiple-valued ferroelectric content-addressable memory

Sheikholeslami, A.; Gulak, P.G.; Hanyu, T.;

Multiple-Valued Logic, 1996. Proceedings., 26th International Symposium on , 1996

Pages: 74 - 79

[Abstract] [PDF Full-Text (416 KB)] IEEE CNF

14 An effective memory addressing scheme for multiprocessor FFT syst Dawoud, D.S.;

Africon Conference in Africa, 2002. IEEE AFRICON. 6th , Volume: 1 , 2-4 Oct. 7 Pages: 29 - 34 vol.1

[Abstract] [PDF Full-Text (385 KB)] IEEE CNF

15 Application specific embedded 8-Port SRAM with simultaneous 256-accessibility

Cheon-Ho Bae; Sun-Ho Chang; Bum-Sik Kim; Lee-Sup Kim; Circuits and Systems, 1999. 42nd Midwest Symposium on , Volume: 2 , 8-11 / Pages:878 - 881 vol. 2

[Abstract] [PDF Full-Text (336 KB)] IEEE CNF

1 2 Next

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ | Terms | Back to Top



Publications/Services Standards Conferences Careers/Jobs Membership

Welcome

	RELEASE 1.8
Help FAQ Terms IEEE	Peer Review Quick Links
Welcome to IEEE Xplore® - Home - What Can i Access? - Log-out	Your search matched 4 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering
Tables of Contents	in the text box.
 Journals & Magazines Conference Proceedings Standards 	memory <and> simultaneous access <and> module Check to search within this result set Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard</and></and>
Search O- By Author O- Basic O- Advanced O- CrossRef	1 Multiaccess memory system for attached SIMD computer Jong Won Park; Computers, IEEE Transactions on , Volume: 53 , Issue: 4 , April 2004 Pages:439 - 452 [Abstract] [PDF Full-Text (1700 KB)] IEEE JNL
Member Services	2 Parallel implementation of motion-compensation for HDTV video dec

- Join IEEE
- Establish IEEE Web Account
- Access the **IEEE Member Digital Library**

IEEE Enterprise

()- Access the **IEEE Enterprise File Cabinet**

Print Format

- ideo dec Lee, C.L.;
- Consumer Electronics, IEEE Transactions on , Volume: 44 , Issue: 2 , May 199 Pages: 251 - 255

[Abstract] [PDF Full-Text (352 KB)]

3 Parallel implementation of motion-compensation for HDTV video dec Lee, C.L.;

ISCE '97 - Proceedings of 1997 IEEE International Symposium on Consumer El 4 Dec. 1997

Pages:51 - 54

[Abstract] [PDF Full-Text (280 KB)]

4 An effective memory addressing scheme for multiprocessor FFT syste Dawoud, D.S.;

Africon Conference in Africa, 2002. IEEE AFRICON. 6th , Volume: 1 , 2-4 Oct. 7 Pages:29 - 34 vol.1

[Abstract] [PDF Full-Text (385 KB)]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top





Welcome
United States Patent and Trademark Office

	RELECASE I.O
Help FAQ Terms IEEE F	Peer Review Quick Links
Welcome to IEEE Xplore® - Home - What Can I Access? - Log-out Tables of Contents	Your search matched 0 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering in the text box.
	memory <and> simultaneous access <and> core Search</and></and>
O- Journals & Magazines	Check to search within this result set
Conference Proceedings Standards	Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard
Search	
O- By Author O- Basic O- Advanced O- CrossRef	Results: No documents matched your query.
Member Services	
O- Join IEEE O- Establish IEEE Web Account O- Access the IEEE Member Digital Library	
IEEE Enterprise	

Print Format

O- Access the

IEEE Enterprise File Cabinet

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top



IEEE Xplore®

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links		
Welcome to IEEE Xplore® - Home - What Can I Access? - Log-out	Your search matched 0 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order. Refine This Search: You may refine your search by editing the current search expression or entering	
Tables of Contents	in the text box.	
O- Journals & Magazines	'memory core' <and> mode <and> interface ☐ Check to search within this result set</and></and>	
Conference Proceedings Standards	Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard	
Search - By Author - Basic - Advanced - CrossRef	Results: No documents matched your query.	
Member Services - Join IEEE - Establish IEEE - Web Account - Access the - IEEE Member - Digital Library - IEEE Enterprise - Access the - IEEE Enterprise - File Cabinet		

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top



IEEE Xplore®

Welcome
United States Patent and Trademark Office

	RELEASE 1.8
Help FAQ Terms IEEE	Peer Review Quick Links
Welcome to IEEE Xplore* - Home - What Can I Access?	Your search matched 6 of 1117580 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order.
C Log-out Tables of Contents	Refine This Search: You may refine your search by editing the current search expression or entering in the text box.
O- Journals & Magazines O- Conference Proceedings	memory core <and> interface Check to search within this result set Results Key:</and>
O- Standards	JNL = Journal or Magazine CNF = Conference STD = Standard
Search O- By Author O- Basic O- Advanced O- CrossRef	1 High-speed DRAM architecture development Ikeda, H.; Inukai, H.; Solid-State Circuits, IEEE Journal of, Volume: 34, Issue: 5, May 1999 Pages: 685 - 692 [Abstract] [PDF Full-Text (608 KB)] IEEE JNL

Member Services

O- Establish IEEE Web Account

O- Join IEEE

O- Access the IEEE Member Digital Library

IEEE Enterprise

- O Access the IEEE Enterprise File Cabinet
- Print Format

2 A hierarchical test methodology for systems on chip

Jin-Fu Li; Hsin-Jung Huang; Jeng-Bin Chen; Chih-Pin Su; Cheng-Wen Wu; Chu Shao-I Chen; Chi-Yi Hwang; Hsiao-Ping Lin; Micro, IEEE, Volume: 22, Issue: 5, Sept.-Oct. 2002

Pages:69 - 81

[Abstract] [PDF Full-Text (396 KB)] IEEE JNL

3 Circuit techniques for 1.5-V power supply flash memory

Otsuka, N.; Horowitz, M.A.;

Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 8 , Aug. 1997

Pages:1217 - 1230

[Abstract] [PDF Full-Text (348 KB)] IEEE JNL

4 A multi-mission space avionics architecture

Chau, S.N.; Reh, K.R.; Cox, B.; Barfield, J.N.; Lockhart, W.L.; McLelland, M.L.; Aerospace Applications Conference, 1996. Proceedings., 1996 IEEE, Volume: 1996

Pages:165 - 176 vol.1

[Abstract] [PDF Full-Text (864 KB)] IEEE CNF

5 A high-speed multi-port data buffer design for low-energy DSP applic Sangjin Hong; Shu-Shin Chin; Fanshi Zhao;

ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International, 12 2001

Pages: 374 - 378

[Abstract] [PDF Full-Text (448 KB)] IEEE CNF

6 A language formalism for verification of PowerPCTM custom memorie compositions of abstract specifications

Bhadra, J.; Martin, A.; Abraham, J.; Abadir, M.; High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEE International , 7-9 Nov. 2001 Pages:134 - 141

[Abstract] [PDF Full-Text (290 KB)] IEEE CNF

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top